REMARKS

The claims are claims 1, 3 and 4.

Claims 1, 3 and 4 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Itoh et al U.S. Patent No. 6,075,941 and Sample et al U.S. Patent No. 5,960,191.

Claim 1 recites subject matter not made obvious by the combination of Itoh et al and Sample et al. Claim 1 recites "selectively assigning control of at least one emulation resource of the integrated circuit to one of said serial scan path or said monitor program." The FINAL REJECTION states at page 3, lines 14 to 18:

> "In fact, Sample (patent 5,960,191) teaches method and system for hardware emulation system including feature of selectively assigning control of emulation resource for circuit emulation system (col. 3. lines 35-49, col. 19, line 48 to col. 24, line 4) and serially scanning path for emulation resource assignment resources as taught in Background of the Invention."

The Applicants respectfully submit that the technique taught in Sample et al differs from the claimed subject matter.

First, Sample et al is directed to a different problem than that claimed. Claim 1 recites a method of "in circuit emulation." This application states at page 3, line 25 to page 4, line 6:

> "Product development and debugging is best handled with an emulation circuit closely corresponding to the actual integrated circuit to be employed in the final product. In circuit emulation (ICE) is in response to this need. An integrated circuit with ICE includes auxiliary circuit not needed in the operating product included solely to enhance emulation visibility. In the typical system level integration circuit, these emulation circuits use only a very small fraction of the number of transistors employed in operating circuits. Thus it is feasible to include ICE circuits in all integrated circuits manufactured. Since every integrated

> circuit can be used for emulation, inventory and manufacturing need not differ between a normal product and an emulation enhanced product."

This portion of the application teaches that in circuit emulation includes circuits manufactured on every integrated circuit used for product development and debugging. In contrast, Sample et al teaches hardware emulation systems for a different purpose. Sample et al states at column 1, lines 11 to 16:

> "Hardware emulation systems are devices designed for verifying electronic circuit designs prior to fabrication as chips or printed circuit boards. These systems are typically built from programmable logic chips (logic chips) and programmable interconnect chips (interconnect chips)."

Verification during circuit design cannot involve in circuit emulation which include circuits in every manufactured integrated circuit. Thus any teaching of Sample et al is inapplicable to this invention.

Second, the teaching of Sample et al do not make obvious the particular selectively assigning control of claim 1. Sample et al states at column 1, line 66 to column 2, line 12:

> "Time-multiplexing is a technique that has been used for sharing a single physical wire or pin between multiple logical signals in certain types of systems where the cost of each physical connection is very high. Such systems include telecommunication systems. Time-multiplexing, however, has not been commonly used in hardware emulation systems such as those available from Quickturn Design Systems, Inc., Mentor Graphics Corporation, Aptix Corporation, and others because the use of prior art time-multiplexing methods significantly reduced the speed at which the emulated circuit could operate. Furthermore, prior art time-multiplexing techniques makes it difficult to preserve the correct asynchronous behavior of an embedded design in the hardware emulation system."

Thus Sample et al teaches his time-multiplexing technique is directed to sharing multiple logical signals on a single physical line. Sample et al fails to teach or suggest that the emulation resources shared on a time basis are selectively assigned to the serial scan path or the emulation monitor as recited in claim 1 Thus Sample et al teaches reassignment of emulation resources in a different context and for a different purpose than claimed. Sample et al fails to teach or suggest the selective assignment claimed. Accordingly, claim 1 is allowable over the combination of Itoh et al and Sample et al.

Claims 3 and 4 are allowable by dependence upon allowable claim 1.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no new search or reconsideration is required.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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